REMARKS

- Claims 1 to 24 are pending in this application
- Claims 1, 5, 9, 13, and 19 to 24 are independent claims

SPECIFICATION AMENDMENTS

The specification has been amended, as required by the Examiner, to update bibliographic information regarding co-pending related applications. No new subject matter has been added.

SECTION 102 REJECTIONS

Claims 5, 8, 13, 16, and 24 stand rejected as anticipated under 35 U.S.C. Section 102(e) by U.S. Patent No. 6,481,251 filed Oct. 25, 1999 and issued to Meier et al. (hereinafter "Meier"). Claim 9 stands rejected as anticipated under 35 U.S.C. Section 102(e) by U.S. Patent No. 6,810,043 filed May 5, 1999 and issued to Naven et al. (hereinafter "Naven"). Applicants respectfully traverse these rejections.

The Examiner appears to be incorrectly equating elements of the references with features recited in Applicant's claims. For example, the Examiner asserts that "examining an empty indicator associated with the scheduling queue" (or the like) as recited in Applicant's Claims 5, 8, 13, 16, and 24 is anticipated by column 13, line 66 to column 14, line 4 of Meier which reads: "If the current tail store queue number is the maximum store queue number value (and thus the increment wraps to zero), the toggle bit of the current store queue number is also inverted. Finally if the empty indication in the empty register indicates that the store queue is empty, the empty

indication is set to indicate not empty (step 90)." The cited passage of Meier appears to be describing a pointer that is reset when the pointer has reached the end of a "store queue" and an indicator that gets "set to indicate not empty" when the pointer has reached the end of the store queue. See the flowchart of Fig. 4, step 90 of Meier. This appears to be distinct from the recited feature of the present invention which involves examining an empty indicator associated with a scheduling queue to determine further action. Unlike the reference, the present invention as recited in Claim 5 is examining an empty indicator to determine whether a scheduling queue should be searched or not. The reference merely describes setting an indicator. More importantly, the empty indication described in Meier does not appear to refer to an indicator that reflects whether data flows are present in a scheduling queue. In other words, the Examiner has not identified, and Applicant cannot find, any teaching or even suggestion within Meier that discloses an indicator that reflects whether data flows are present in a scheduling queue. Thus, since this feature of Applicant's claims is not present in the Meier reference, Applicant respectfully requests withdrawal of the Section 102 rejection of Claims 5, 8, 13, 16, and 24.

The Examiner further asserts that "refraining from searching the scheduling queue if the empty indicator indicates that the scheduling queue is empty" and "searching the scheduling queue if the empty indicator indicates that the scheduling queue is not empty" (or the like) as recited in Applicant's Claims 5, 8, 13, 16, and 24 is anticipated by column 14, line 60 to 67 of Meier which reads: "Store queue control circuit 74 generates a mask

using the load's store queue number and the head store queue number (step 120). The mask includes a bit for each store queue entry. The bit is set if the store queue entry is eligible to be hit by the load (i.e. the entry is between the head entry indicated by the head store queue number and the entry indicated by the load's store queue number), and is clear if the store queue entry is not eligible to be hit by the load." The cited passage of Meier appears to describe generating a mask that is used to indicate whether an entry is located between two other entries ("the head entry" and "the entry indicated by the load's store queue number"). This appears to be quite distinct from the recited feature of the present invention which involves determining whether a scheduling queue should be searched or not. Thus, since this feature of Applicant's claims is not present in the Meier reference, Applicant respectfully requests withdrawal of the Section 102 rejection of Claims 5, 8, 13, 16, and 24 for this additional reason.

The Examiner further asserts that "detaching from the scheduling queue a winning flow found in the searching step" (or the like) as recited in Applicant's Claims 5, 8, 13, 16, and 24 is anticipated by column 15, line 7 to 10 of Meier which reads: "In other words, store queue control circuit 74 determines if there is still a hit signal asserted after masking via step 122. If so, data is forwarded to D-cache 44 from the hit entry (step 126)." The cited passage of Meier appears to describe a data transfer from an entry depending on whether the entry is located between two other entries ("the head entry" and "the entry indicated by the load's store queue number"). This appears to be distinct from the recited feature of the

present invention which involves dequeuing a data flow found in the searching step. Thus, since this feature of Applicant's claims is not present in the Meier reference, Applicant respectfully requests withdrawal of the Section 102 rejection of Claims 5, 8, 13, 16, and 24 for this additional reason.

Further, more generally, Meier appears to describe an instruction pipeline for a processor. In contrast, the claims of the present invention are directed to processing data "flows" (*e.g.*, "dequeuing a flow" as recited in Claim 5). Therefore, for the above reasons, Applicant respectfully requests withdrawal of the Section 102 rejections of Claims 5, 8, 13, 16, and 24.

Regarding Claim 9, the Examiner asserts that Naven teaches "placing an empty indicator associated with the scheduling queue in a condition to indicate that the scheduling queue is not empty" as recited in Applicant's Claim 9. The Examiner quotes a portion of column 8, lines 19 to 28 in support of his assertion. The full passage reads: "the master snoop memory 20 is N bits wide such that each N-bit word 22 thereof corresponds to one of the **groups of N consecutive storage locations 2. Each bit within such an N-bit word 22 corresponds individually to one of the** storage locations 2 of the group. In this case, when a bit in the word 22 is set to 1, this denotes that the corresponding storage location 2 has at least one VC entered therein. **If the bit is 0, on the other hand, this denotes that the corresponding storage location 2 is 'empty', i.e. does not contain a valid entry.**" The bold text was omitted by the Examiner. Despite the term 'empty', the reference appears to merely describe an array of valid/invalid bits for consecutive storage locations

that may hold one ore more "VCs" or "virtual channels." Thus, the reference does not appear to describe setting an empty/non-empty indicator for data flows in a scheduling queue. Thus, since this feature of Applicant's claim is not present in the Naven reference, Applicant respectfully requests withdrawal of the Section 102 rejection of Claim 9.

SECTION 103 REJECTIONS

Claims 1 to 4, 19 and 21 stand rejected under 35 U.S.C. Section 103 as unpatentable over Applicant's Figs. 1 to 3 in view of Meier. Claims 10 to 12, 17, 18, and 23 stand rejected under 35 U.S.C. Section 103 as unpatentable over Naven in view of the Examiner's assertion of what would have been obvious. Claims 6 and 14 stand rejected under 35 U.S.C. Section 103 as unpatentable over Meier in view of an article written by Lyons et al. entitled "Estimating Clock Speeds for the ATMSWITCH Architechture", Proc. Networks '99 (The Third New Zealand ATM and Broadband Workshop), 21-22 Jan. 1999, pps 39-53 (hereinafter "Lyons"). Claims 7 and 15 stand rejected under 35 U.S.C. Section 103 as unpatentable over Meier in view of Lyons and Naven. Claim 20 stands rejected under 35 U.S.C. Section 103 as unpatentable over Applicant's Figs. 1 to 3 in view of Meier and Naven. Claims 22 and 24 stand rejected under 35 U.S.C. Section 103 as unpatentable over Meier in view of the Examiner's assertion of what would have been obvious. Applicants respectfully traverse these rejections.

Regarding each of the claims rejected at least in part based on Meier (*i.e.*, Claims 1 to 4, 6, 7, 14, 15, 19 to 22, and 24), Applicant asserts that the Examiner's Section 103 rejections of these claims are untenable

because neither Meier (as discussed above with respect to the Section 102 rejections) nor the other relied upon references teach or suggest the features that the Examiner asserts are taught by Meier. Thus, for this reason, Applicant respectfully requests withdrawal of the Section 103 rejections of Claims 1 to 4, 6, 7, 14, 15, 19 to 22, and 24.

Further, regarding each of the claims rejected at least in part based on Naven (*i.e.*, Claims 7, 10 to 12, 15, 17, 18, 20, and 23), Applicant asserts that the Examiner's Section 103 rejections of these claims are untenable because neither Naven (as discussed above with respect to the Section 102 rejection) nor the other relied upon references teach or suggest the features that the Examiner asserts are taught by Naven. Thus, for this reason, Applicant respectfully requests withdrawal of the Section 103 rejections of Claims 7, 10 to 12, 15, 17, 18, 20, and 23.

Regarding Claims 1, 3, 19, 20, and 21 in particular, in addition to the reason noted above, Applicant asserts that the Examiner's Section 103 rejections of Claims 1, 3, 19, 20, and 21 are further untenable because the Examiner has not provided a proper motivation to combine the art described in Applicant's Background section with Meier. Even if Meier taught Applicant's claimed empty indicator, which it does not, the only motivation to make the combination provided by the Examiner is that a cycle may be wasted without an empty indicator. This motivation comes directly from Applicant's specification and is not suggested by the reference. The Examiner has not provided any reasoning suggesting that this benefit would have occurred to one of ordinary skill

at the time of the invention. There appears to be nothing in the references or the Examiner's reasoning that suggests a benefit from (or desire to) preventing a wasted cycle. Thus, absent a proper motivation, Applicant asserts that the Examiner has failed to establish a *prima facie* case of obviousness, and therefore the rejections of Claims 1, 3, 19, and 21 are untenable for this additional reason. Applicant respectfully requests withdrawal of the Section 103 rejections of Claims 1, 3, 19, 20, and 21 for this additional reason.

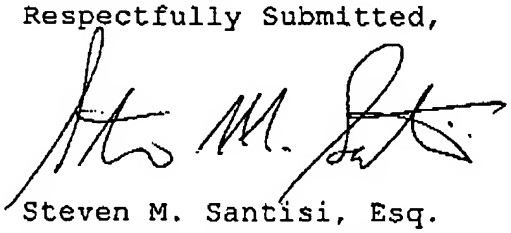
Regarding Claim 10, the Examiner asserts that Naven "provides the motivation for a need for a formula to effectively calculate the NST [next scheduled time to transmit a cell]." The Examiner further asserts that "it should be obvious to incorporate the well known weighted fair queue technique (CP + (WF x FS)/SF) disclosed by the applicant into the scheduling circuitry to schedule cell transmission including a master calendar and slave calendar disclosed by Naven in order to effectively calculate the NST." Applicants do not accept these assertions and respectfully request the Examiner to provide a reference in support. If the Examiner is relying on Official Notice, Applicant respectfully requests the Examiner provide an affidavit in support of his assertions. Absent support, Applicant asserts that the Examiner has not established a *prima facie* case of obviousness and respectfully requests withdrawal of the Section 103 rejection of Claim 10 for this additional reason.

CONCLUSION

The Applicant believes all the claims are in condition for allowance, and respectfully request reconsideration and allowance of the same.

A Request for Extension of Time is enclosed herewith, with authorization to charge any extension fee to Deposit Account No. 04-1696. Applicant does not believe any other Request for Extension of Time is required but if it is, please accept this paragraph as an additional Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696. Applicant does not believe any other fees are due regarding this amendment. If any other fees are required, however, please charge Deposit Account No. 04-1696. The Applicant encourages the Examiner to telephone Applicant's attorney should any issues remain.

Respectfully Submitted,



Steven M. Santisi, Esq.
Registration No. 40,157
Dugan & Dugan, PC
Attorneys for Applicants
(914) 332-9081

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Tarrytown, New York